DG485

Octal Analog Switch Array

Features

- Low On-Resistance: 55 Ω
- Rail-to-Rail Analog Input Range
- Serial Interface
- Low-Power—P_D: 35 nW
- TTL and CMOS Compatible
- Any Combination of 8 SPST to the Output
- High Speed—t_{ON}: 170 ns

Benefits

- Low Signal Distortion
- Devices Can Be Chained for System Expansion
- Reduced Board Space
- Reduced Switch Errors
- Reduced Power Supply Requirements
- Simple Interfacing

Applications

- Audio Switching and Routing
- Audio Teleconferencing
- Data Acquisition and Industrial Process Control
- Battery Powered Remote Systems
- Automotive, Avionics and ATE Systems
- Summing Amplifiers

Description

The DG485 is an analog switch array consisting of eight SPST switches connected to a common output. This device may be used as an 8-channel multiplexer in serial control applications. Any, all or none of the eight switches may be closed at any given time. Combining low on-resistance ($r_{DS(on)}$ 55 Ω, typ.) and fast switching (t_{ON}: 170 ns, typ.), the DG485 is ideally suited for data acquisition, process control, communication, and avionic applications.

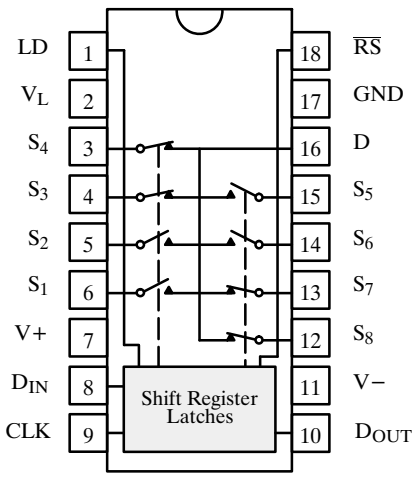
Control data is input serially into the shift register with each clock pulse. The shift register contents can be latched-in (via LD) at any point into an octal latch which in turn controls all switches. $\overline{RS}$ resets the shift register, forcing all latch inputs to a low condition (all switches off). The serial input (D_{IN}) and serial output (D_{OUT}) allow daisy chaining of multiple arrays for large systems.

Built on the Siliconix high voltage silicon gate process the DG485 has a wide 44-V power supply voltage rating. An epitaxial layer prevents latchup.

Each channel conducts equally well in either direction when on and blocks up to rail-to-rail voltages when off.

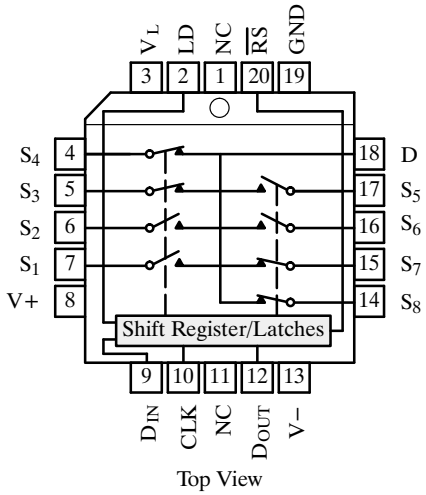
Functional Block Diagrams and Pin Configurations

Dual-In-Line



Top View

PLCC and LCC



Top View

Truth Tables and Ordering Information

$\overline{RS}$	CLK*	D_{IN}	D_1	D_n
1	↑	0	0	D_{n-1}
1	↑	1	1	D_{n-1}
1	↓	X	D_1	D_n (No Change)
0	X	X	0	0

*CLK Input Edge Triggered

LD*	D_n	L_n	SW_n
↑	0	0	OFF
↑	1	1	ON
↓	D_n	L_n	(No Change)

*LD Input Level Triggered

Ordering Information

Temp Range	Package	Part Number
−40 to 85°C	18-Pin Plastic DIP	DG485DJ
	20-Pin PLCC	DG485DN
−55 to 125°C	LCC-20	DG485AZ/883

Absolute Maximum Ratings

Voltages Referenced to V−
V+ . . . . . 44 V
GND . . . . . 25 V
Digital Inputs[a] V_S, V_D . . . . . (V−) −2 V to (V+) + 2 V
or 30 mA, whichever occurs first
Continuous Current (Any Terminal) . . . . . 30 mA
Current, S or D (Pulsed 1 ms, 10% duty cycle) . . . . . 100 mA
Storage Temperature (AZ Suffix) . . . . . −65 to 150°C
(DJ, DN Suffix) . . . . . −65 to 125°C

Power Dissipation (Package)[b]
18-Pin Plastic DIP[c] . . . . . 470 mW
20-Pin PLCC, LCC[d] . . . . . 800 mW

Notes:
a. Signals on S_X, D_X or IN_X exceeding V+ or V− will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads soldered or welded to PC board.
c. Derate 6 mW/°C above 75°C.
d. Derate 10 mW/°C above 75°C.

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C		D Suffix −40 to 85°C		Unit
					Min[d]	Max[d]	Min[d]	Max[d]	
Analog Switch									
Analog Signal Range[e]	V_{ANALOG}		Full		−15	15	−15	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	V+ = 13.5 V, V− = −13.5 V I_S = −5 mA, V_D = ±10 V	Room Full	55		85 125		85 125	Ω
Delta Drain-Source On-Resistance[g]	$\Delta r_{DS(on)}$		Room	6					%
Switch Off Leakage Current	$I_{S(off)}$	V+ = 16.5 V, V− = −16.5 V V_D = ∓15.5 V, V_S = ±15.5 V	Room Full	0.01	−1 −20	1 20	−1 −10	1 10	nA
	$I_{D(off)}$		Room Full	0.1	−10 −200	10 200	−10 −50	10 50	
Channel On Leakage Current	$I_{D(on)}$	V± = ±16.5 V V_S = V_D = ±15.5 V One Switch At A Time	Room Full	0.11	−20 −500	20 500	−20 −50	20 50	
		V± = ±16.5 V, V_S = V_D = ±15.5 V All Switches On	Room	0.2					
Input									
Input Current with V_{IN} Low	I_{IL}	V_{IN} Under Test = 0.8 V All Other = 2.4 V	Room Full	−0.000 1	−1 −5	1 5	−1 −5	1 5	µA
Input Current with V_{IN} High	I_{IH}	V_{IN} Under Test = 2.4 V All Other = 0.8 V	Room Full	0.0001	−1 −5	1 5	−1 −5	1 5	
Serial Data Output									
Output Voltage with V_{IN} Low − D_{OUT}	V_{OL}	I_O = 1.6 mA, V+ = 4.5 V	Full	0.25		0.4		0.4	V
Output Voltage with V_{IN} High − D_{OUT}	V_{OH}	I_O = −80 µA, V+ = 16.5 V V_L = 4.75 V	Full	4.4	2.7		2.7		
Dynamic Characteristics									
Turn-On Time	t_{ON}	V_S = ±10 V See Figures 1, 8	Room Full	170		200 275		200 275	ns
Turn-Off Time	t_{OFF}	V_S = ±10 V See Figures 2, 3, 8	Room Full	150		200 275		200 276	
Data Setup Time	t_{DS}	See Figures 4, 8	Room Full		40 60		40 60		
Data Hold Time	t_{DH}		Room Full		40 60		40 60		
LOAD Hold Time	t_{LH}	See Figures 5, 8	Room Full		100 150		100 150		
$\overline{\text{RESET}}$ Hold Time	t_{RH}		Room Full		100 150		100 150		
$\overline{\text{RESET}}$ ↑ to $\overline{\text{CLOCK}}$ ↑ Delay	t_{DRC}		Room Full		40 60		40 60		
Charge Injection	Q	V_S = 0 V, C_L = 1,000 pF Any One Channel	Room	17					pC
Off Isolation[e]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz See Figure 9	Room	−75					dB

DG485

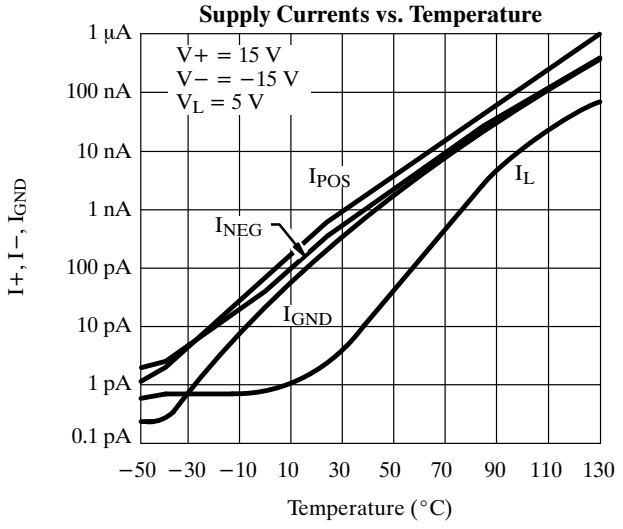
Specifications[a]

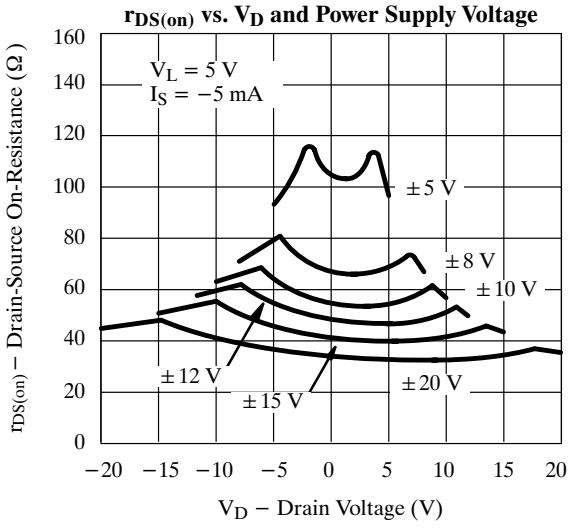
Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V V_L = 5 V, V_{IN} = 2.4 V, 0.8 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Dynamic Characteristics (Cont'd)									
Maximum Clock Frequency	f_{CLK}		Room	10					MHz
Source Off Capacitance[e]	$C_{S(off)}$	V_{gen} = 0 V, R_{gen} = 0 Ω, f = 1 MHz	Room	7					pF
Drain Off Capacitance[e]	$C_{D(off)}$		Room	43					pF
On-State Capacitance[e]	$C_{D(on)}$	V_{gen} = 0 V, R_{gen} = 0 Ω, f = 1 MHz One Channel On	Room	53					pF
		V_{gen} = 0 V, R_{gen} = 0 Ω, f = 1 MHz All Channels On	Room	122					pF
Power Supplies									
Positive Supply Current	I+	V+ = 16.5 V, V− = −16.5 V V_{IN} = 0 or 5 V, V_L = 5.25 V D_{OUT} Open	Room Full	0.001		3 10		3 10	µA
Negative Supply Current	I−		Room Full	−0.001	−3 −10		−3 −10		µA
Logic Supply Current	I_L		Room Full	0.001		3 10		3 10	µA
Ground Current	I_{GND}		Room Full	−0.001	−3 −10		−3 −10		µA

Notes:
a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.
g.

$$\text{For each } V_D: \quad \Delta r_{DS(on)} = \left(\frac{r_{DS(on)}\ \text{MAX} - r_{DS(on)}\ \text{MIN}}{r_{DS(on)}\ \text{AVE}} \right)$$

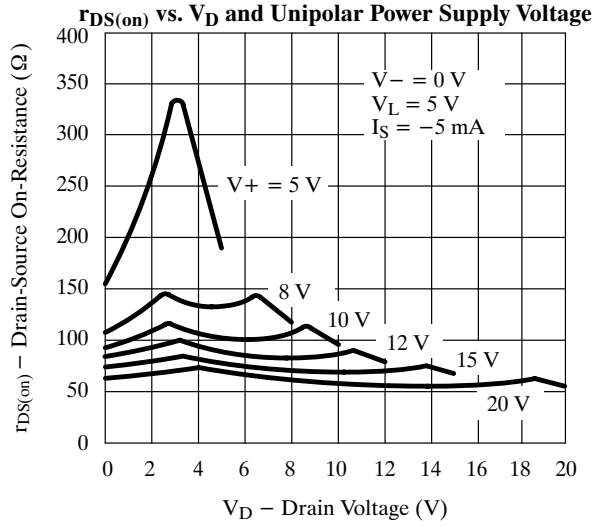
Typical Characteristics



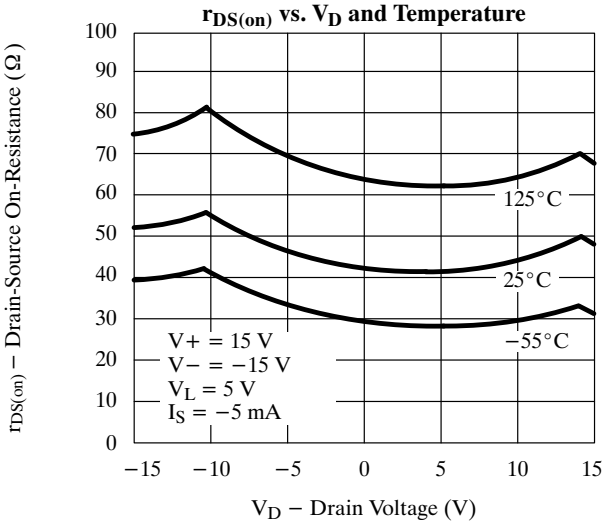


Typical Characteristics (Cont'd)

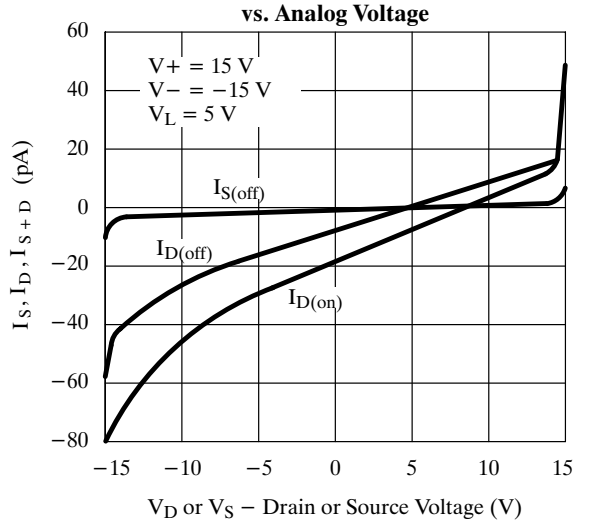
$r_{DS(on)}$ vs. V_D and Unipolar Power Supply Voltage



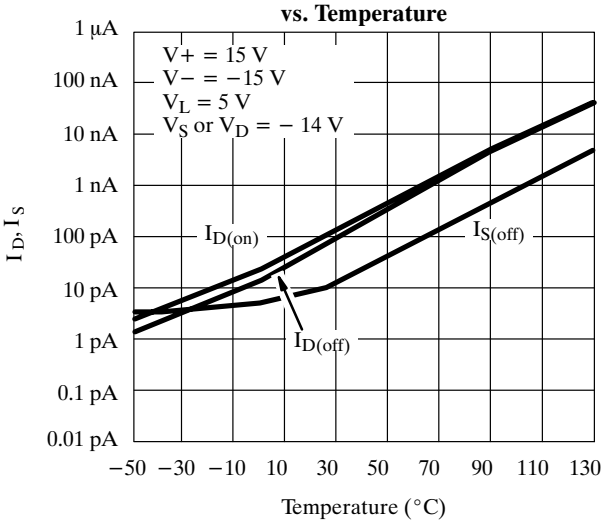
$r_{DS(on)}$ vs. V_D and Temperature



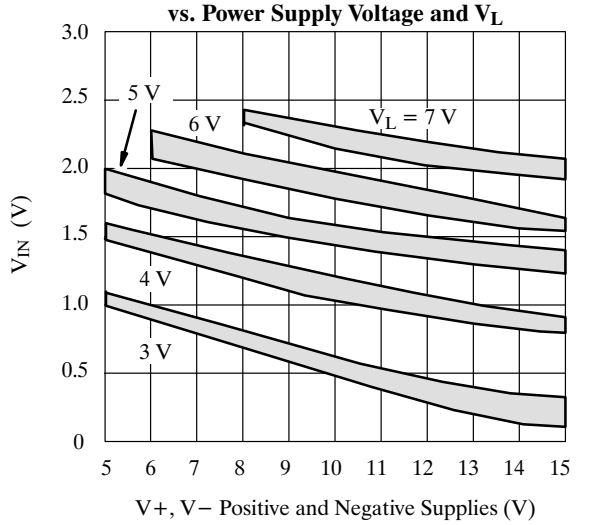
Channel On/Off Leakage Currents vs. Analog Voltage



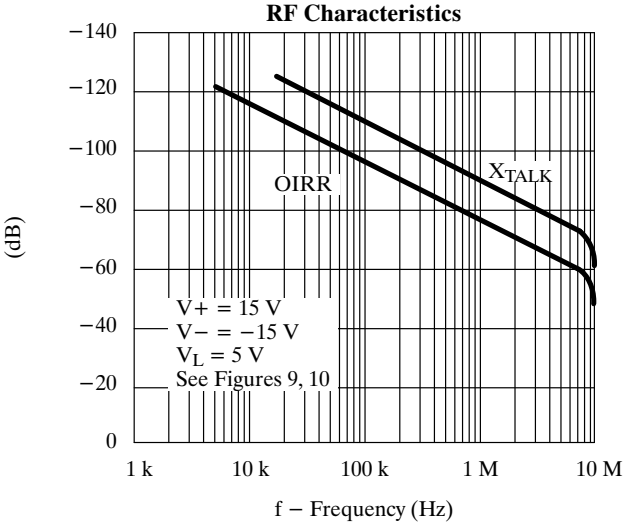
Channel On/Off Leakage Currents vs. Temperature



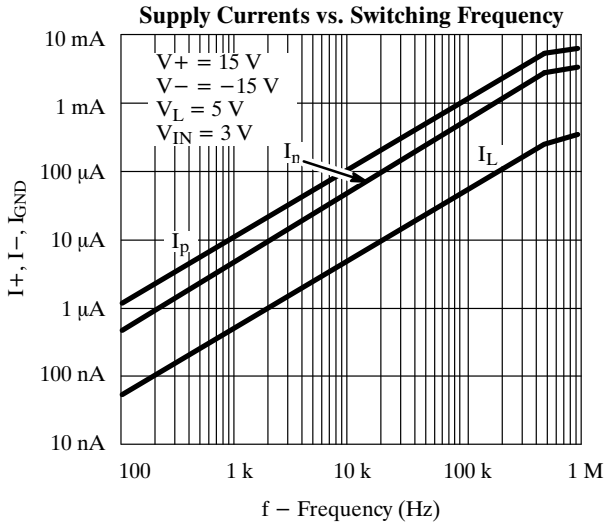
Switching Threshold vs. Power Supply Voltage and V_L

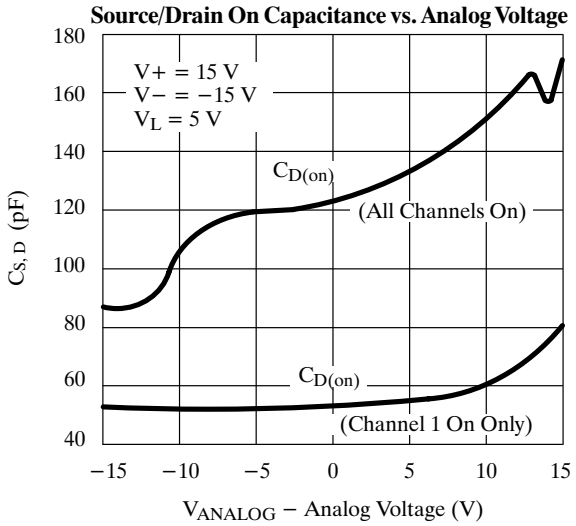


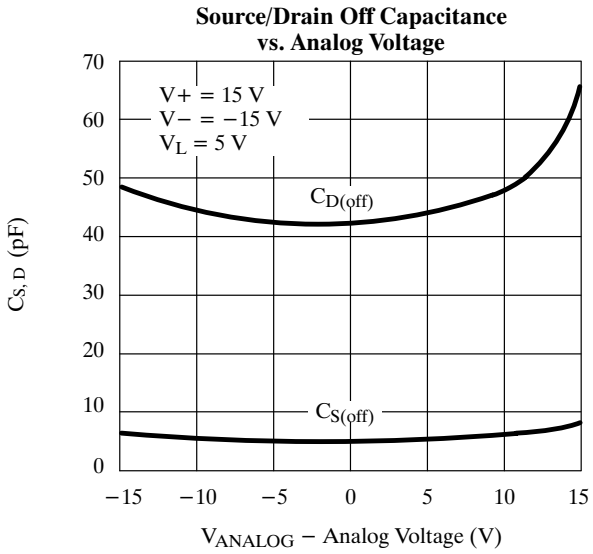
RF Characteristics

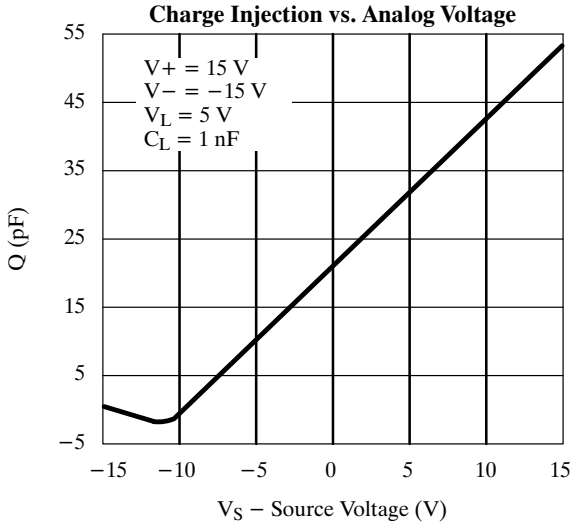


Typical Characteristics (Cont'd)









Timing Diagrams

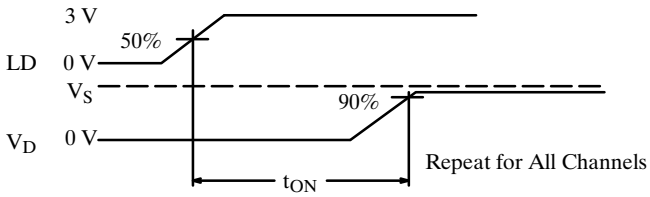


Figure 1. t_{ON} from LD

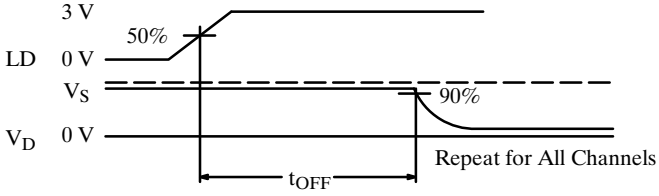


Figure 2. t_{OFF} from LD

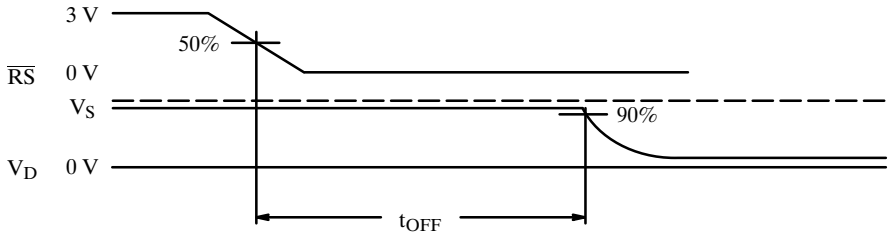


Figure 3. t_{OFF} from $\overline{RS}$

Timing Diagrams (Cont'd)

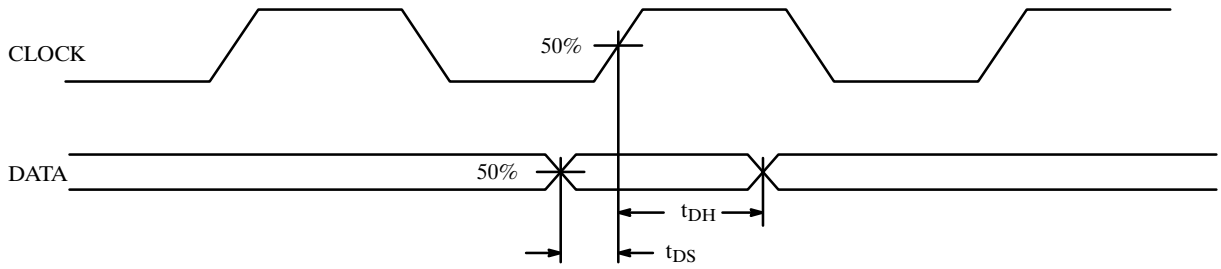


Figure 4. Data Setup and Hold Time

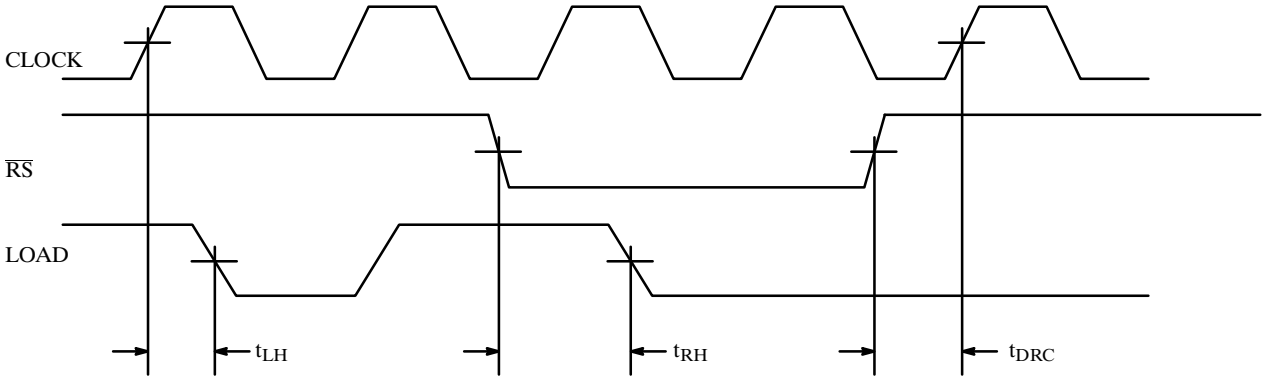
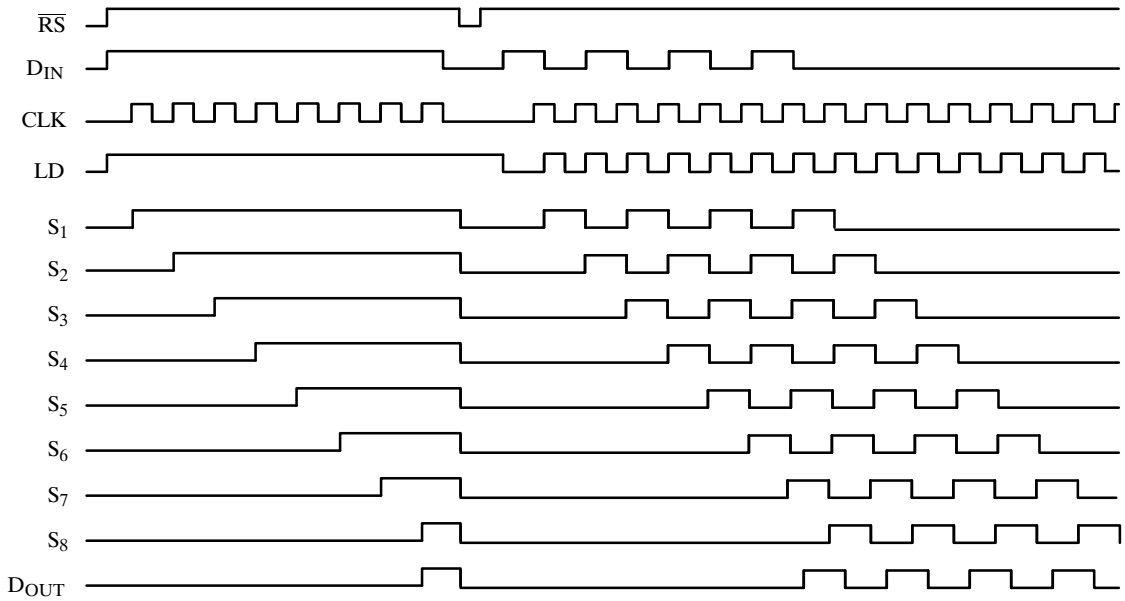


Figure 5. Timing Relationships



$S_1 - S_8$ and D_{OUT} are expected output with the drain connected high. The sources require pull-down of 1 kΩ

Figure 6.

Schematic Diagram (Typical Channel)

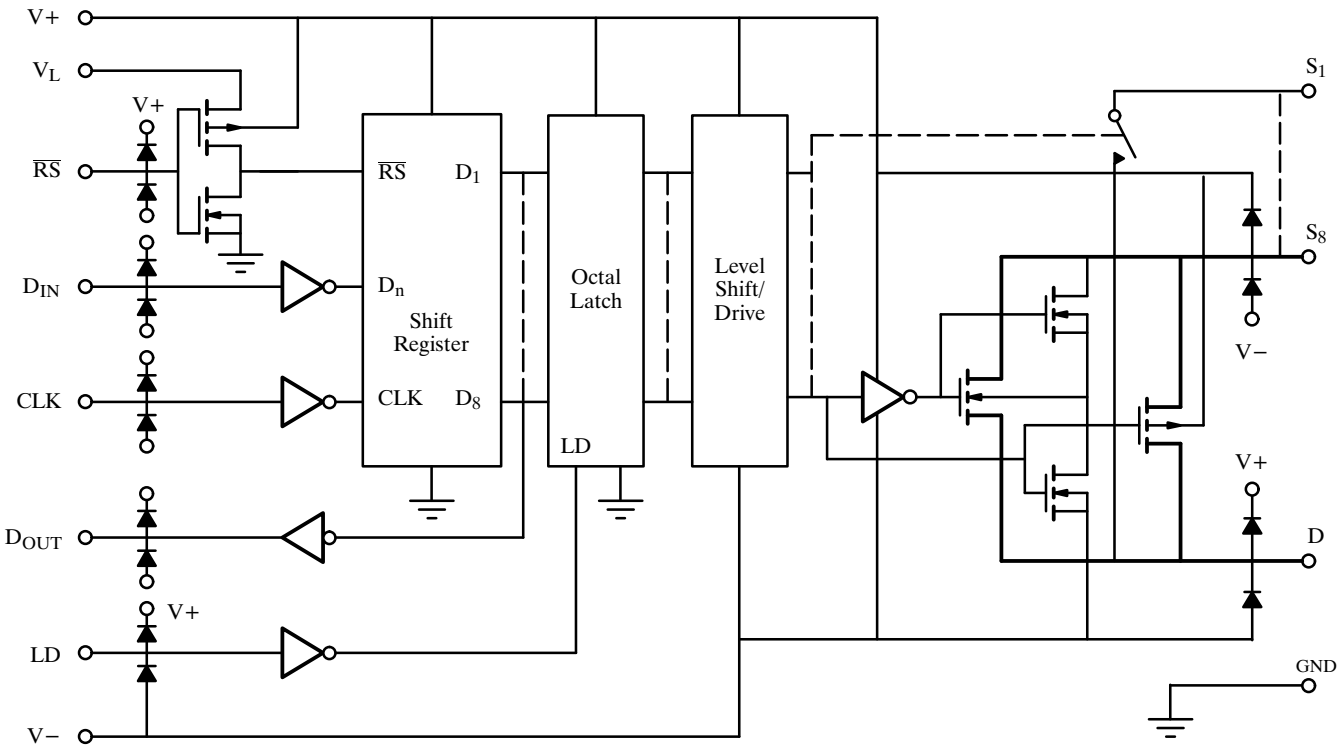


Figure 7.

Test Circuits

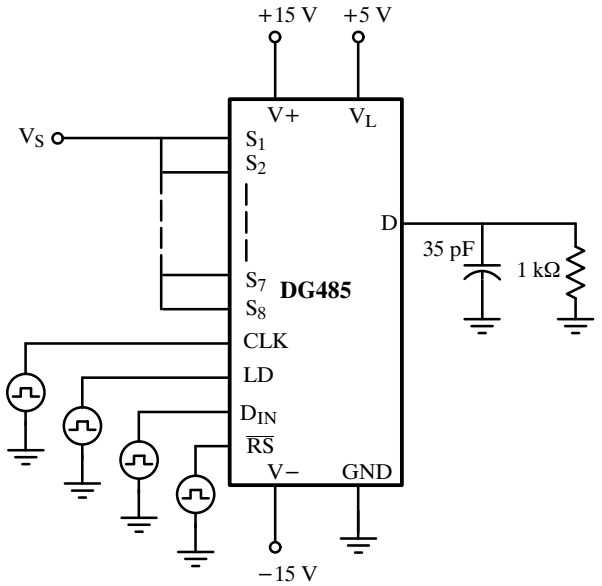


Figure 8. Switching Time Test Circuit

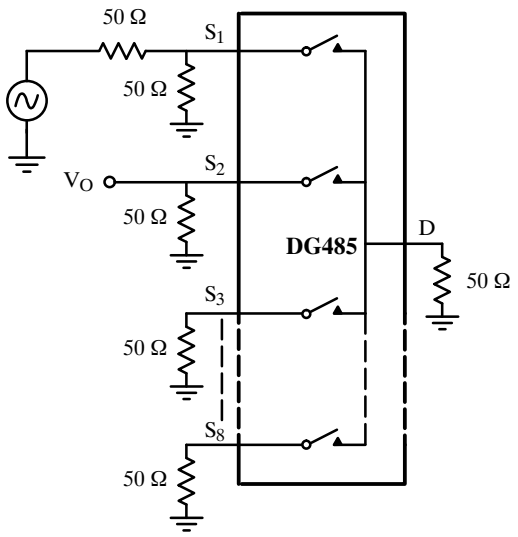


Figure 9. Adjacent Input Crosstalk

Test Circuits

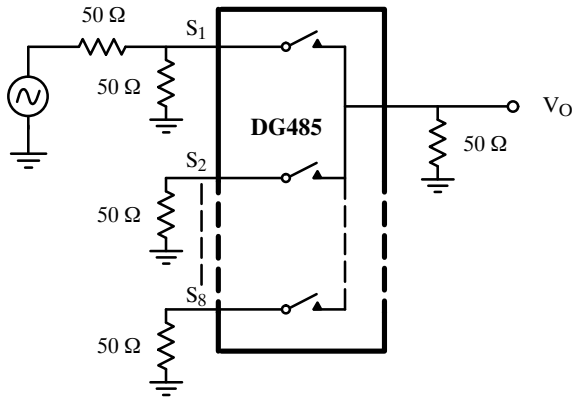
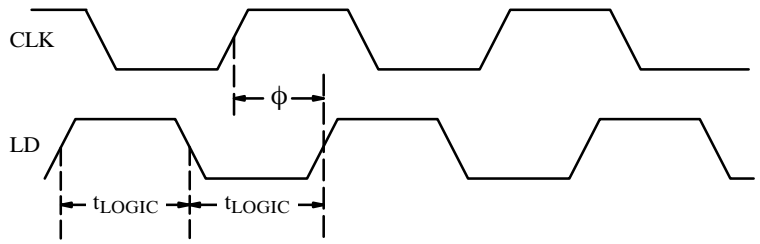


Figure 10. Off Isolation

Applications



ϕ= for CLK and LD inputs of the same frequency. The recommended phase delay of LD from CLK is ½ t_{LOGIC} to t_{LOGIC}:

$t_{LOGIC(MIN)}$: 80 ns at 25°C, 150 ns at 125°C

V+ = 15 V
V− = −15 V
GND = 0 V

Figure 11.

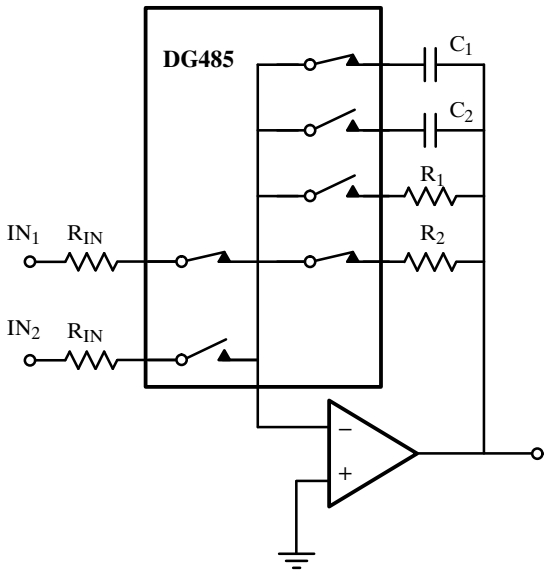


Figure 12. Multi-Function Circuit Provides Input Selection, Gain Ranging and Filtering with One DG485

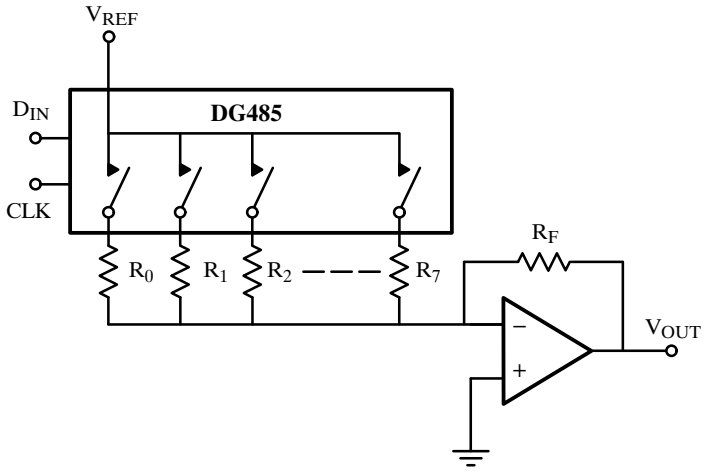


Figure 13. Serial DAC Circuit

Applications (Cont'd)

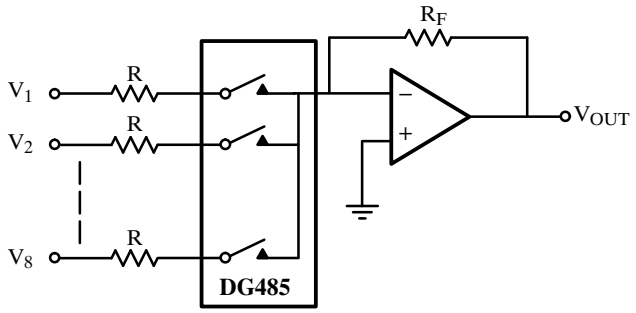


Figure 14. Summing Node Mixer

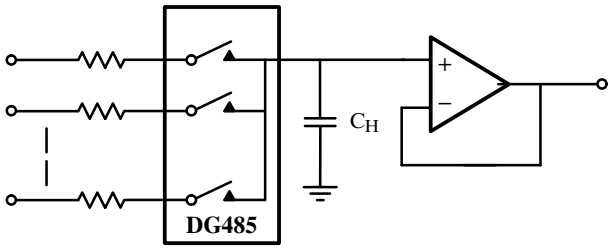


Figure 15. Multiplexing, Sampling Application

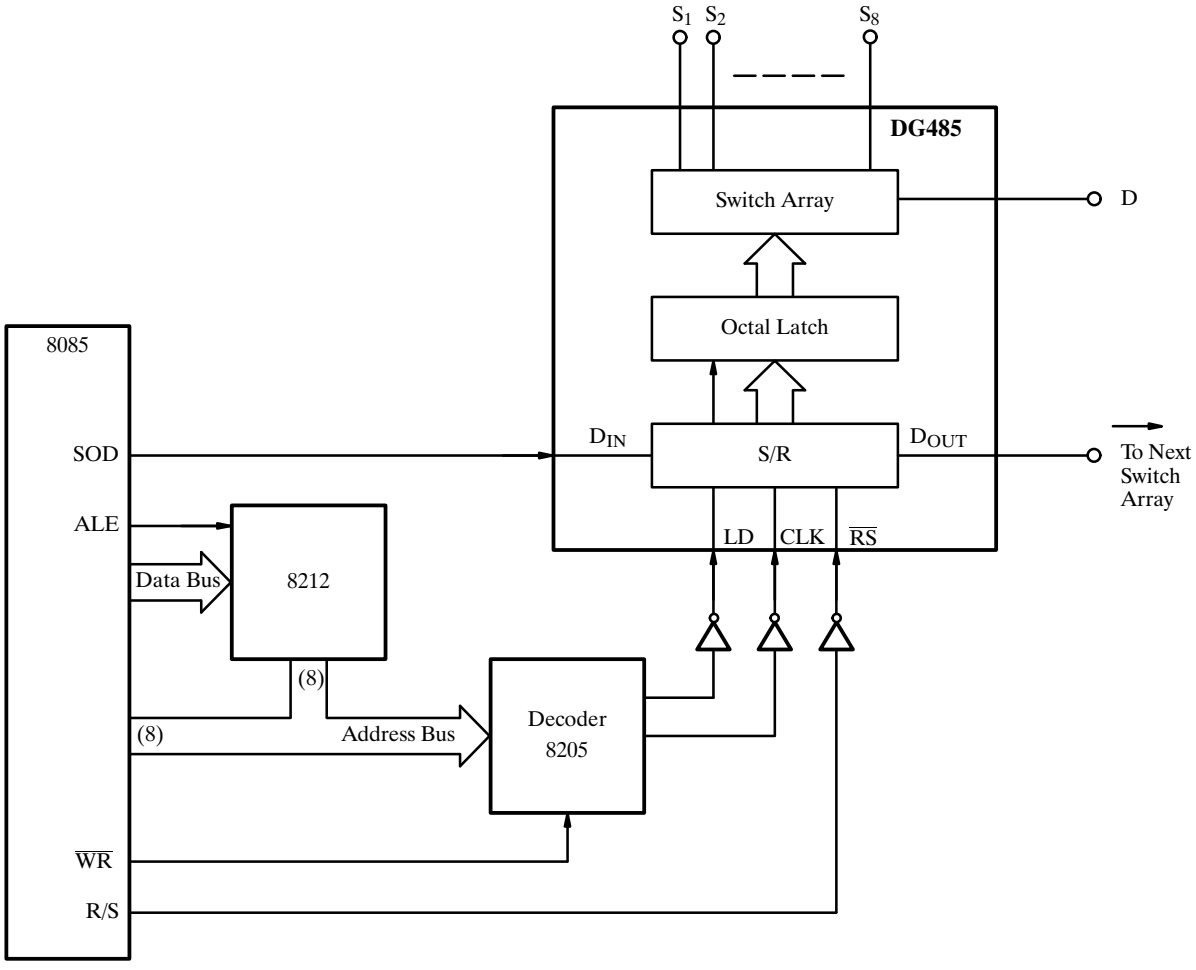


Figure 16. Direct Serial Interface (8085)